WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device that has a structure in which a plurality of unit FETs are arranged in a line, the method comprising the steps of:

(a) determining in advance a number 'p' of said unit FETs in which a desired drain current value is obtained in the semiconductor device, and forming 'm' active layer regions more than said number 'p' so as to be arranged in a line on a substrate;

(b) forming a gate electrode, a source electrode, and a drain electrode, respectively on each of said 'm' active layer regions, thereby forming basic structures of said 'm' unit FETs;

(c) predicting a drain current value of said semiconductor device from a value obtained by measuring a drain current value of one of said basic structures, and comparing the predicted value with said desired drain current value, thereby determining the number 'n' of said basic structures that satisfies the desired drain current value;

(d) forming an inter-layer insulating film on said basic structure; and

(e) forming simultaneously a first contact hole that penetrates the inter-layer insulating film, and that exposes part of a surface of said gate electrode; a second contact hole that penetrates said inter-layer insulating film, and that exposes part of a surface of said source electrode; and a third contact hole that penetrates said inter-layer insulation layer, and that exposes part of a surface of said drain electrode,

wherein said first, second and third contact holes are formed for only a region

of 'n' basic structures of said inter-layer insulating film,

provided that $m \geqq n$, and $m, n > 0$.

2. A method according to claim 1,

wherein the number 'n' of said basic structures is a minimum number 'n' that satisfies the equation $I_{dss} \times n/m \geqq I_{dss\ design}$ where said predicted value is defined as I_{dss}, and said desired drain current value is defined as $I_{dss\ design}$.

3. A method according to claim 1,

wherein the step (e) of forming said first, second , and third contact holes comprises the sub-steps of:

(i) forming a resist film on said inter-layer insulating film;

(ii) employing a mask having provided thereon a window for forming contact holes corresponding to each of said first, second, and third contact holes formed in a region of said inter-layer insulating film of each of said basic structures, thereby carrying out the sub-step of carrying out exposure and developing for said resist film while said mask is shifted by one of said basic structures at a time to form a resist pattern having 'n' contact hole patterns; and

(iii) employing said resist pattern, thereby carrying out an etching process of said inter-layer insulating film.

4. A method of fabricating a semiconductor device that has a structure in which a plurality of unit FETs are arranged in a line, the method comprising the steps of:

(a) determining in advance a number 'p' of said unit FETs in which a desired drain current value is obtained in the semiconductor device,

and forming 'm' active layer regions more than said number 'p' so as

to be arranged in a line on a substrate;

(b) forming a gate electrode, a source electrode, and a drain electrode, respectively on each of said 'm' active layer regions, thereby forming basic structures of said 'm' unit FETs;

(c) predicting a drain current value of said semiconductor device from a measured value obtained by measuring a drain current value of each of said basic structures, and comparing the predicted value with said desired drain current value, thereby determining the number 'n' of said basic structures that satisfies the desired drain current value;

(d) forming an inter-layer insulating film on said basic structure;

(e) simultaneously forming a first contact hole that penetrates the inter-layer insulating film, and that exposes part of a surface of said gate electrode; a second contact hole that penetrates said inter-layer insulating film, and that exposes part of a surface of said source electrode; and a third contact hole that penetrates said inter-layer insulating film, and that exposes part of a surface of said drain electrode;

(f) the pad forming step of forming a gate pad each in said first contact hole and on said inter-layer insulating film, forming a source pad each in said second contact hole and on said inter-layer insulating film, forming a first drain pad each in said third contact hole and on said inter-layer insulating film, and forming a second drain pad on said inter-layer insulating film, the second drain pad being spaced apart from said first drain pad; and

(g) forming an air bridge wiring that connects said first drain pad and said second drain pad to each other,

wherein said pad forming step is carried out for a region of said 'n' basic

structures of said inter-layer insulating film,

provided that $m \geqq n$, and $m, n > 0$.

5. A method according to claim 4, wherein the number 'n' of said basic structure is a minimum number 'n' that satisfies the equation $I_{dss} \times n/m \geqq I_{dss\ design}$ where said predicted value is defined as I_{dss}, and said desired drain current value is defined as $I_{dss\ design}$.

6. A method according to claim 4, wherein said pad forming step (f) comprises the sub-steps of:

(i) forming a resist film on said inter-layer insulating film;

(ii) employing a pad pattern mask that has a pattern of said gate pad, source pad, first drain pad, and second drain pad and a pad erasing mask that has a pattern which is configured so as to enclose a predetermined pad forming region on each one of basic structures other than said 'n' basic structures, thereby exposing said resist film, and then, developing the film to form a pad forming resist pattern; and

(iii) employing the pad forming resist pattern, thereby forming said gate pad, source pad, first drain pad, and second drain pad by means of a lift-off method.

7. A method according to claim 6, wherein exposure of said resist film is carried out by a two-step exposure with a first exposure employing said pad pattern mask and a second exposure employing said pad erasing mask.

8. A method according to claim 4, wherein said pad forming step (f) comprises the sub-steps of:

(i) forming a resist film on said inter-layer insulating film;

(ii) employing a pad pattern mask that has a pattern of said gate pad,

source pad, first drain pad, and second drain pad and a slit pattern mask that divides regions on the said 'n' basic structure and on non-'n' basic structure, thereby exposing said resist film, and then, developing the film to form a pad forming resist pattern; and

(iii) employing the pad forming resist pattern, thereby forming said gate pad, source pad, first drain pad, and second drain pad by means of a lift-off method.

9. A method according to claim 8,

wherein exposure of said resist film is carried out by a two-step exposure with a first exposure employing said pad pattern mask and a second exposure employing said slit pattern mask.

10. A method of fabricating a semiconductor device that has a structure in which a plurality of unit FETs are arranged in a line, the method comprising the steps of:

(a) designing in advance a number 'p' of said unit FETs in which a desired drain current value is obtained in the semiconductor device,

and then, forming 'm' active layer regions more than said number 'p' so as to be arranged in a line on a substrate;

(b) forming a gate electrode, a source electrode, and a drain electrode, respectively, on each of said 'm' active layer regions, thereby forming basic structures of said 'm' unit basic structures;

(c) dividing said 'm' basic structures into 'x' unit FET blocks composed of a plurality of basic structures;

(d) predicting a drain current value of said semiconductor device to be obtained by measuring a drain current value of one of said basic structures,

and comparing the predicted value with said desired drain current value, thereby determining the number 'y' of said unit FET blocks in which said desired drain current value is obtained;

(e) forming an inter-layer insulating film on said 'x' unit FET blocks;

(f) forming simultaneously a first contact hole that penetrates the inter-layer insulating film, and that exposes part of a surface of said gate electrode, a second contact hole that penetrates said inter-layer insulating film, and that exposes part of a surface of said source electrode, and a third contact hole that penetrates the inter-layer insulating film, and that exposes part of a surface of said drain electrode;

(g) forming a gate pad in said first contact hole and on said inter-layer insulating film of each of said unit FET blocks, forming a source pad each in said second contact hole and on said inter-layer insulating film of each of said unit FET blocks, forming a first drain pad in said third contact hole and on said inter-layer insulating film, and forming a second drain pad on said inter-layer insulating film, the second drain pad being spaced apart from said first drain pad in said unit FET blocks; and

(h) forming a first pad wiring that connects said first drain pad and said second drain pad to each other, and then, forming a second pad wiring that connects said 'y' of the 'x' gate pads, source pads, and second drain pads with each other, respectively,

wherein $0 < m$, $0 < x$, $y < m$, and $y < x$.

11. A method according to claim 10, wherein the number 'y' of said unit FET blocks is the number determined from the minimum number 'n' of basic structures that satisfies the equation $I_{dss} \times n/m \geqq I_{dss\ design}$ where said

predicted value is defined as I_{dss}, and said desired drain current value is defined as $I_{dss\ design}$.

12. A method of fabricating a semiconductor device that has a structure in which a plurality of unit FETs are arranged in a line, the method comprising the steps of:

(a) defining as 'p' the number of said unit FETs in which a desired drain current value is obtained in the semiconductor device,
forming basic structures of 'm' unit FETs which is more than the 'p', measuring a drain current value of one of the basic structures, and then, predicting from the measured value a drain current value of a semiconductor device after it is fabricated;

(b) comparing said predicted value with said desired drain current value, thereby determining the number 'n' of basic structures in which the desired drain current value is obtained.

13. A method according to claim 12, wherein a wiring pattern is formed for said 'n' basic structures.

14. A method according to claim 12, wherein there is provided a characteristic chart that shows a relationship between a drain current value of each of the basic structures at a time when the basic structures of the semiconductor fabricated by employing similar fabricating methods are formed; and a drain current value of the semiconductor device after is fabricated,

and wherein a value uniquely obtained by causing said measured value to correspond to the characteristic chart is defined as said predicted value.